( ) Preliminary Specifications
(V) Final Specifications

Module	**13.3”(13.28”) WXGA Color TFT-LCD with LED Backlight design**
Model Name	**B133EW07 V2 (H/W:0A)**
Note ( )	***LED Backlight without driving circuit design***

Customer	**Date**	**Approved by**	**Date**
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		Kevin Shen	2/25/2010
Note: This Specification is subject to change without notice.		**NBBU Marketing Division / AU Optronics corporation**	

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Record of Revision

Version and Date	Page	Old description	New Description	Remark
1.0 2010/2/25	All	Final spec		

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostic breakdown.

2. General Description

B133EW07 V2 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the WXGA (1280(H) x 800(V)) screen and 262k colors (RGB 6-bits data driver) without LED backlight driving circuit. All input signals are LVDS interface compatible.

B133EW07 V2 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	337.8 ,13.3W"(13.28)			
Active Area	[mm]	286.08 X178.8			
Pixels H x V		1280x3(RGB) x 800			
Pixel Pitch	[mm]	0.2235X0.2235			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally White			
White Luminance **(Note: ILED is LED current)**	[cd/m^2]	330 typ. 300min ILED=23 mA @94% duty cycle			
Luminance Uniformity		50 max. (160 points)			
Contrast Ratio		500 typ, 400min			
Response Time	[ms]	8 typ / 16 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	4.36 W @ Black (typical, the logic plus the backlight @94% duty cycle @23mA, 3.3V forward bias voltage)			
Weight	[Grams]	300typ., 310 max.			
Physical Size	[mm]		Min.	Typ.	Max.
		Length	-	297.15	-
		Width	-	203.15	-
		Thickness	-	-	3.6
Electrical Interface		1 channel LVDS			
Glass Thickness	[mm]	0.5			
Surface Treatment		Glare, Hardness 3H,			

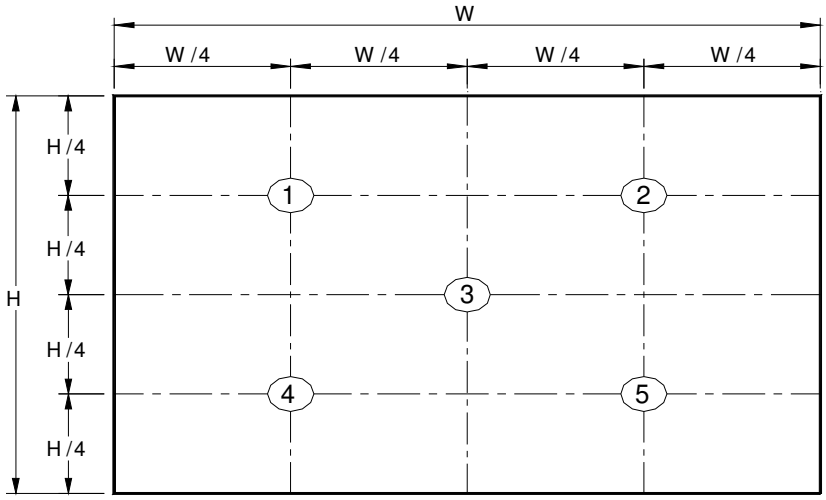
Support Color		262K colors (RGB 6-bit)
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

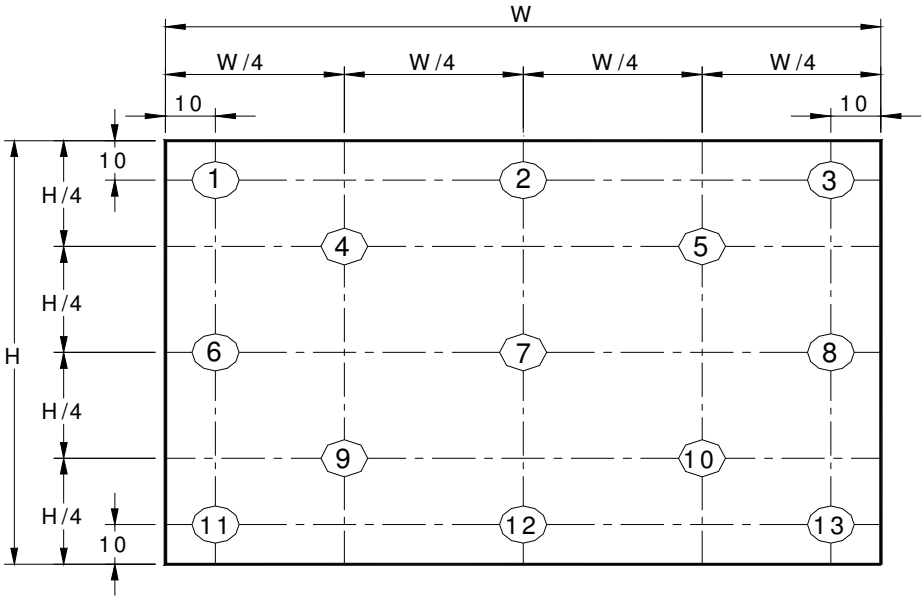
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance			160 points average	300	330	-	cd/m^2	1, 4, 5.
Viewing Angle		θ_R	Horizontal (Right) CR = 10	65	70	-	degree	4, 9
		θ_L		65	70	-		
		ϕ_H	Vertical (Upper) CR = 10	40	45	-		
		ϕ_L	(Lower)	50	55	-		
Luminance Uniformity		δ_{160P}	160 Points	50	-	-		2, 3, 4
Contrast Ratio		CR		400	500	-		4, 6
Cross talk		%	Optical			2.0		4, 7
Response Time		T_r	Rising	-	-	-	msec	4, 8
		T_f	Falling	-	-	-		
		T_{RT}	Rising + Falling	-	16	25		
Color / Chromaticity Coodinates	Red	Rx	CIE 1931	0.620	0.640	0.660		4
		Ry		0.315	0.330	0.345		
	Green	Gx		0.290	0.310	0.330		
		Gy		0.590	0.610	0.630		
	Blue	Bx		0.120	0.150	0.170		
		By		0.040	0.060	0.080		
	White	Wx		0.297	0.313	0.329		
		Wy		0.313	0.329	0.345		
NTSC		%		-	72	-		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

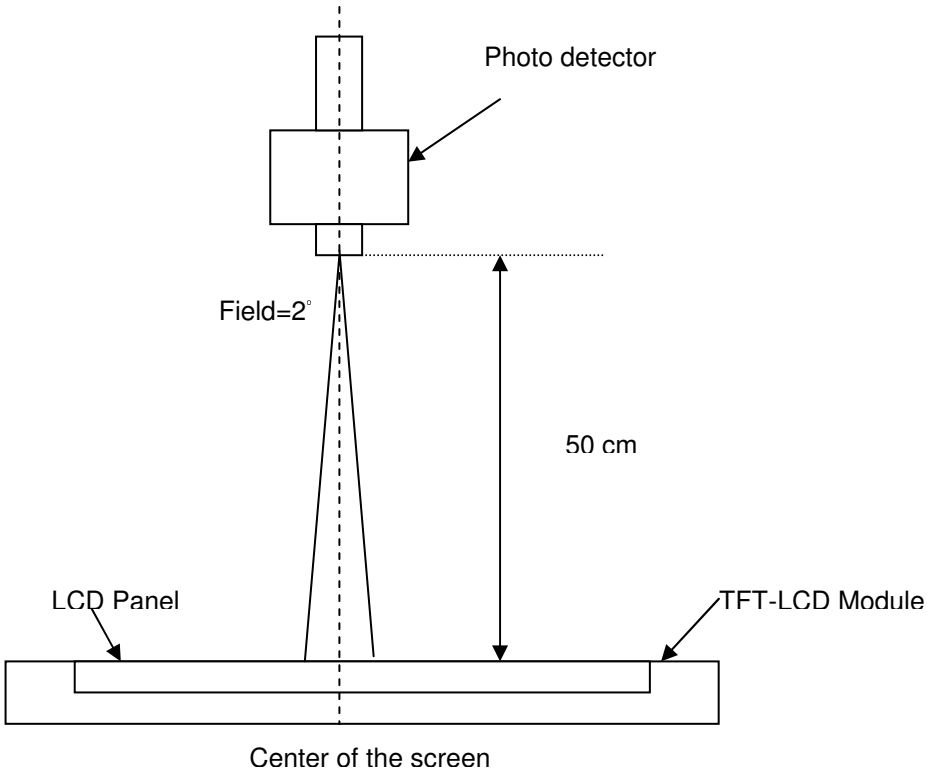
$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting

Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

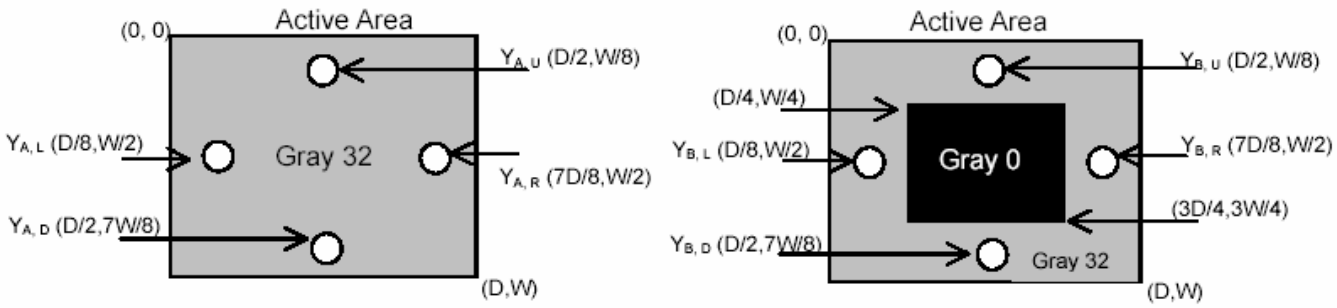
Note 7： Definition of Cross Talk (CT)

$CT = | Y_B - Y_A | / Y_A \times 100$ (%)

Where

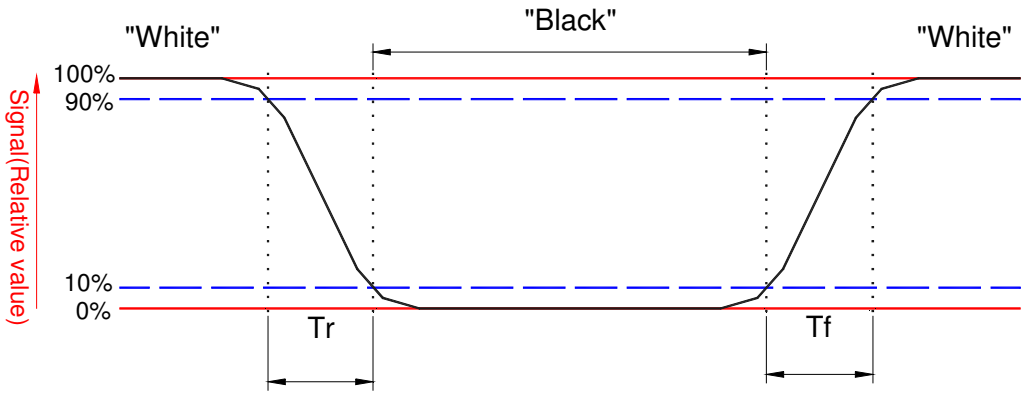
Y_A = Luminance of measured location without gray level 0 pattern (cd/m2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m2)



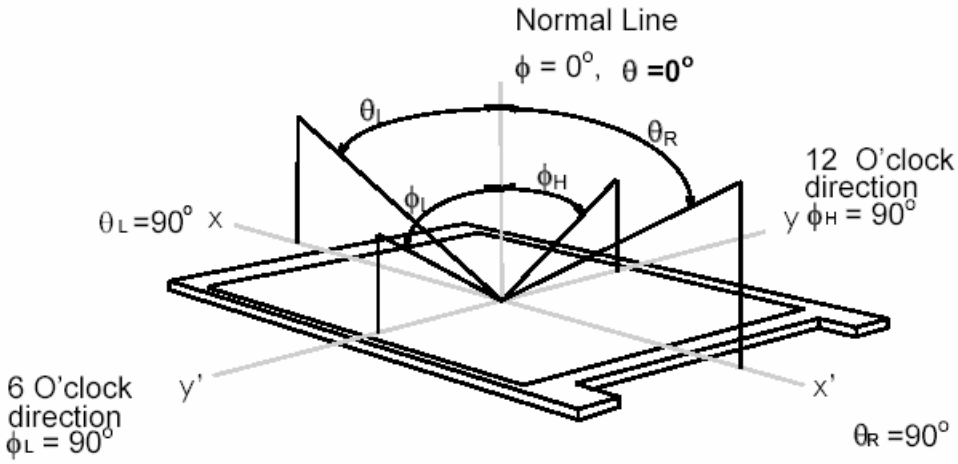
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



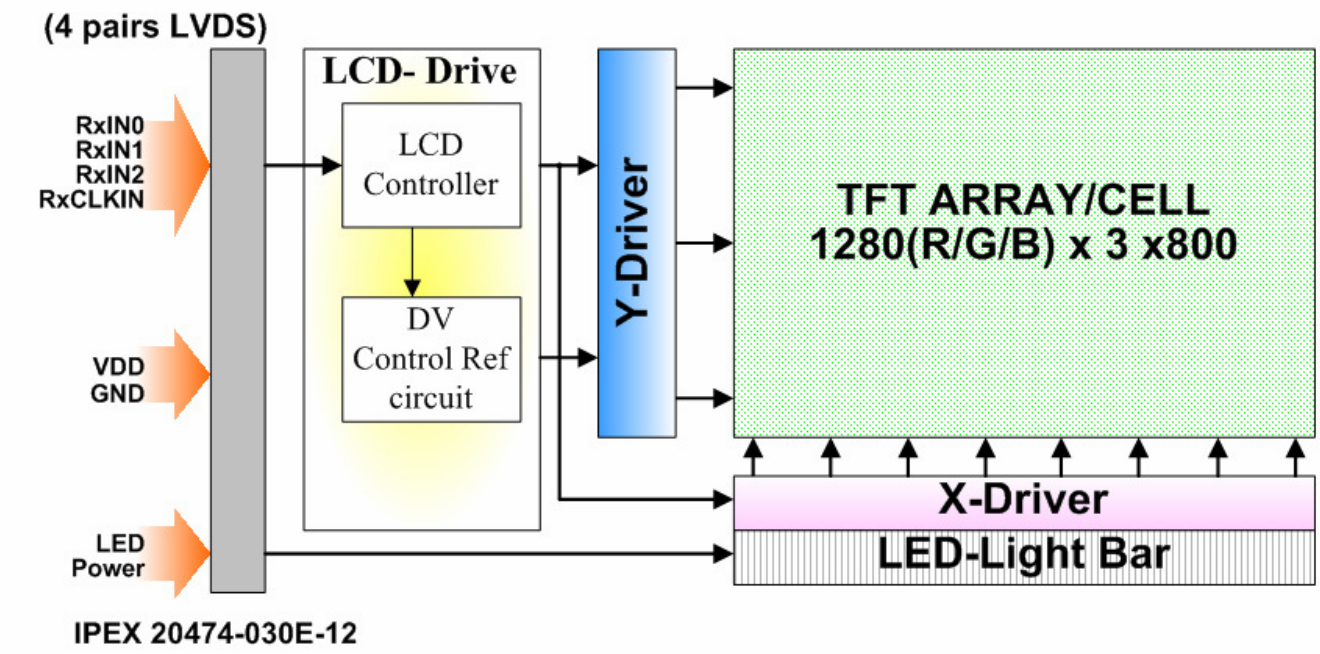
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram
sho
ws the functional block of the 13.3 inches wide Color TFT/LCD 30 Pin (One CH/connector Module)



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

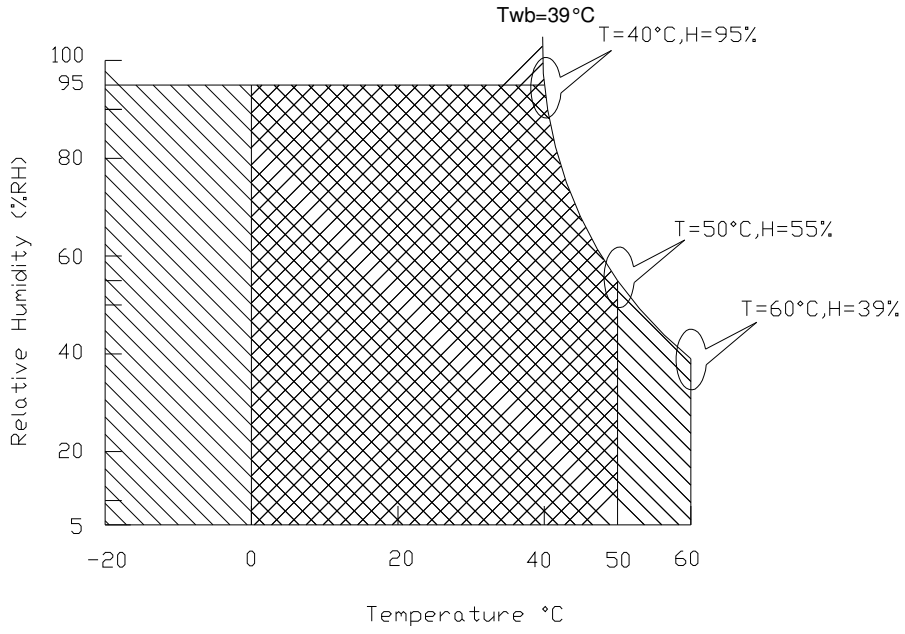
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range Storage Range +

5. Electrical characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

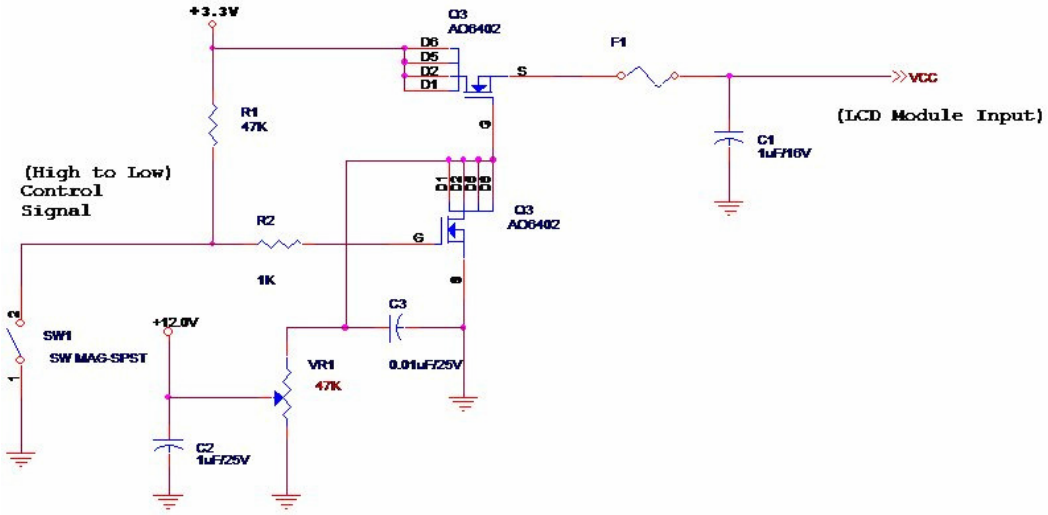
Input power specifications are as follows;

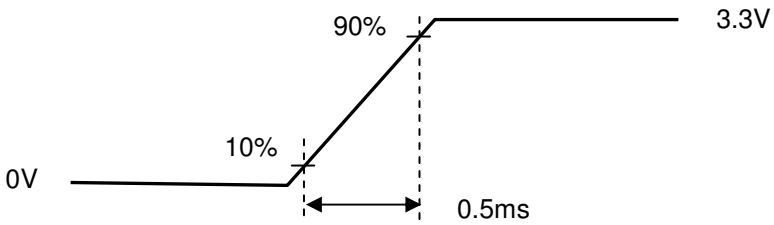
The power specification are measured under 25℃ and frame frenquency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	0.9	[Watt]	Note 1
IDD	IDD Current	-	220	250	[mA]	Note 1
IRush	Inrush Current	-	700	1500	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : Black Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3} \times I_{black}$)

Note 2 : Measure Condition





Vin rising time

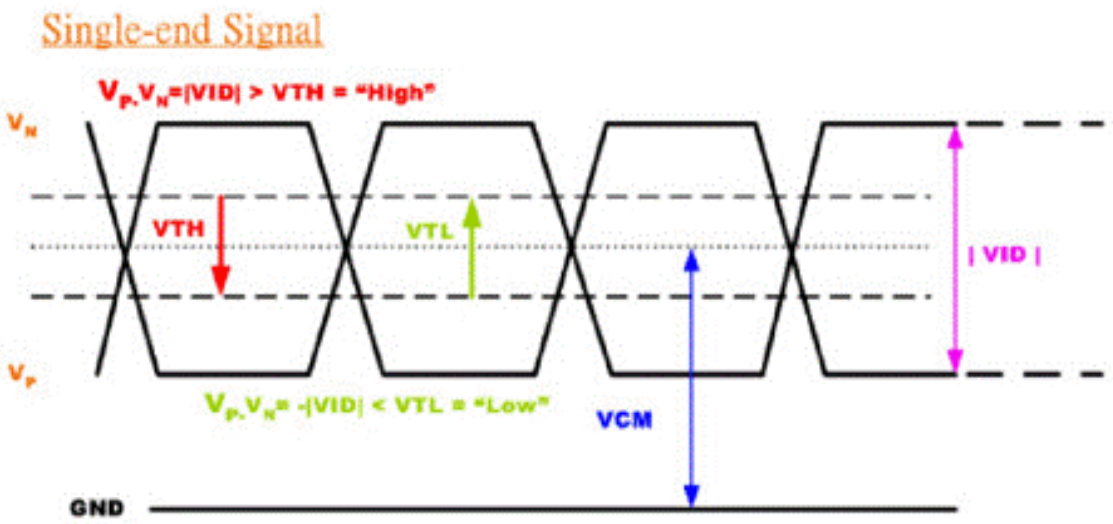
5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
V_{TH}	Differential Input High Threshold (Vcm=+1.2V)		+100	[mV]
V_{TL}	Differential Input Low Threshold (Vcm=+1.2V)	-100	-	[mV]
V_{CM}	Differential Input Common Mode Voltage	0.8	2.0	[V]

Note: LVDS Signal Waveform



5.2 Backlight Unit

Parameter guideline for LED

LED Parameter guideline for LED driving selection (Ref. Remark 1)

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	--	--	3.2	[Watt]	(Ta=25℃)
LED Forward Current	IF	--	20	30	[mA]	(Ta= 25℃)
LED Power consumption	P_{LED}	--	4	--	[Watt]	(Ta=25℃) Note 1
LED Life-Time	N/A	10,000	--	--	Hour	(Ta=25℃), Note 2 I_F=20 mA
Output PWM frequency	F_{PWM}	100	200	20K	Hz	
Duty ratio @20kHZ	--	5	--	100	%	

Note 1: Calculator value for reference P_{LED} = V_F (Normal Distribution) * I_F (Normal Distribution) / Efficiency

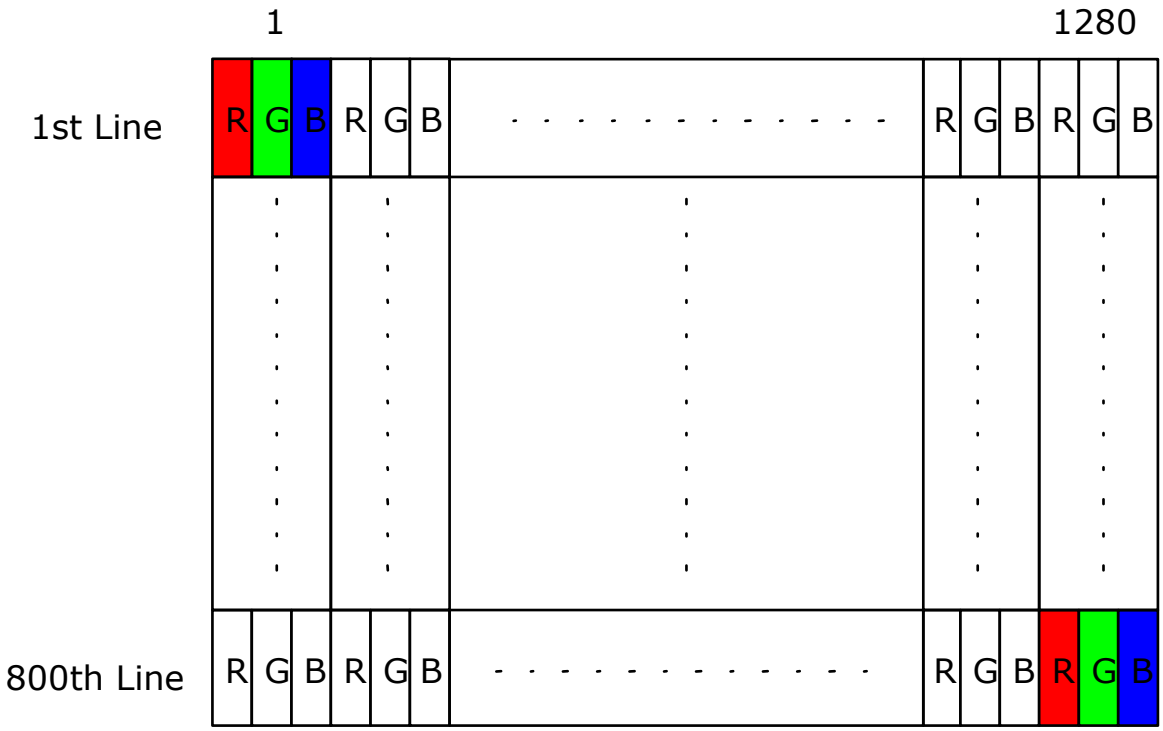
Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

Note 3: Totally using 54 Led bins

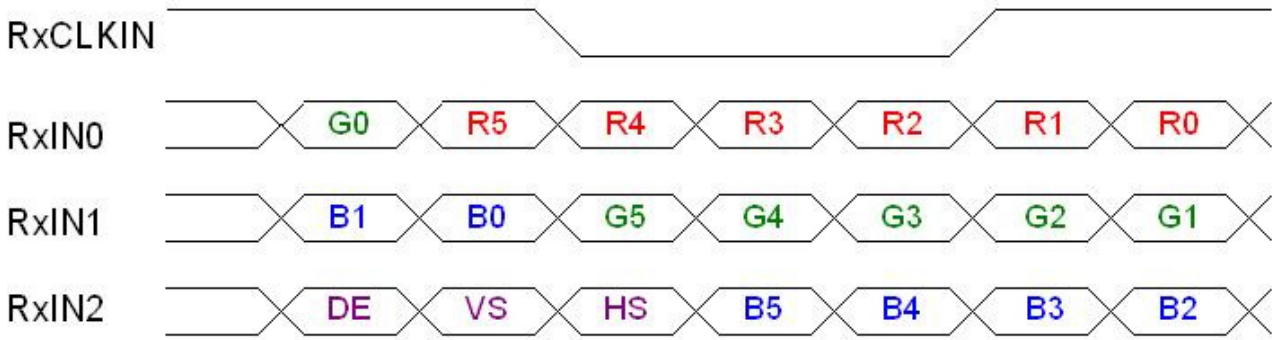
6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The input data format



Signal Name	Description	
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) Red-pixel Data	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
G5 G4 G3 G2 G1 G0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) Green-pixel Data	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) Blue-pixel Data	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
RxCLKIN	Data Clock	The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high.
DE	Display Timing	This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	The signal is synchronized to RxCLKIN .
HS	Horizontal Sync	The signal is synchronized to RxCLKIN .

Note: Output signals from any system shall be low or High-impedance state when VDD is off.

6.3 Integration Interface and Pin Assignment

6.3.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	IPEX or compatible
Type / Part Number	IPEX 20474-030E-12 or compatible
Mating Housing/Part Number	IPEX 20472-030E-12 or compatible

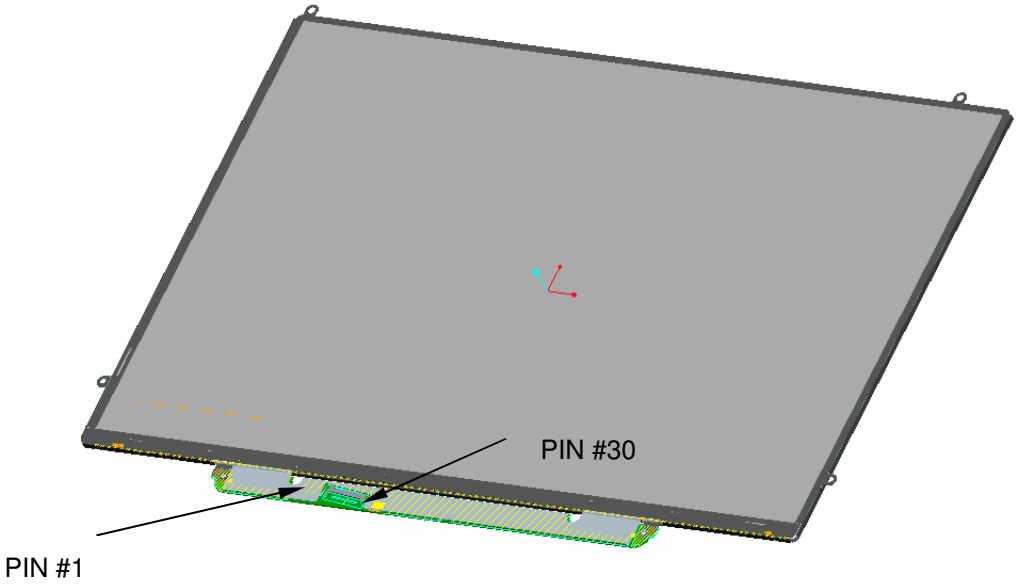
6.3.2 Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

Pin	Symbol	Description
1	GND	Ground
2	Vcc	Power Supply (+3.3V)
3	V_{analog}	Power Supply (+3.3V)
4	V_{EDID}	DDC Power +3.3V
5	Vsync	Vsync
6	Clk_{EDID}	DDC Clock
7	$DATA_{EDID}$	DDC Data
8	Rin0-	Differential Data Input
9	Rin0+	Differential Data Input
10	GND	Ground
11	Rin1-	Differential Data Input
12	Rin1+	Differential Data Input
13	GND	Ground
14	Rin2-	Differential Data Input
15	Rin2+	Differential Data Input
16	GND	Ground
17	Clkin-	Differential Clock Input
18	Clkin+	Differential Clock Input
19	GND	Ground
20	NC	NC
21	Vdc(1 &2)	LED Annold (Positive)
22	Vdc(3&4)	LED Annold (Positive)

23	NC	NC
24	Vdc1	LED Cathode (Negative)
25	Vdc2	LED Cathode (Negative)
26	Vdc3	LED Cathode (Negative)
27	Vdc4	LED Cathode (Negative)
28	Vdc5	LED Cathode (Negative)
29	Vdc6	LED Cathode (Negative)
30	NC	NC

Note: Connector Diagram



6.4 Interface Timing

6.4.1 Timing Characteristics

Basically, interface timings should match the 1280x800 /60Hz manufacturing guide line timing.

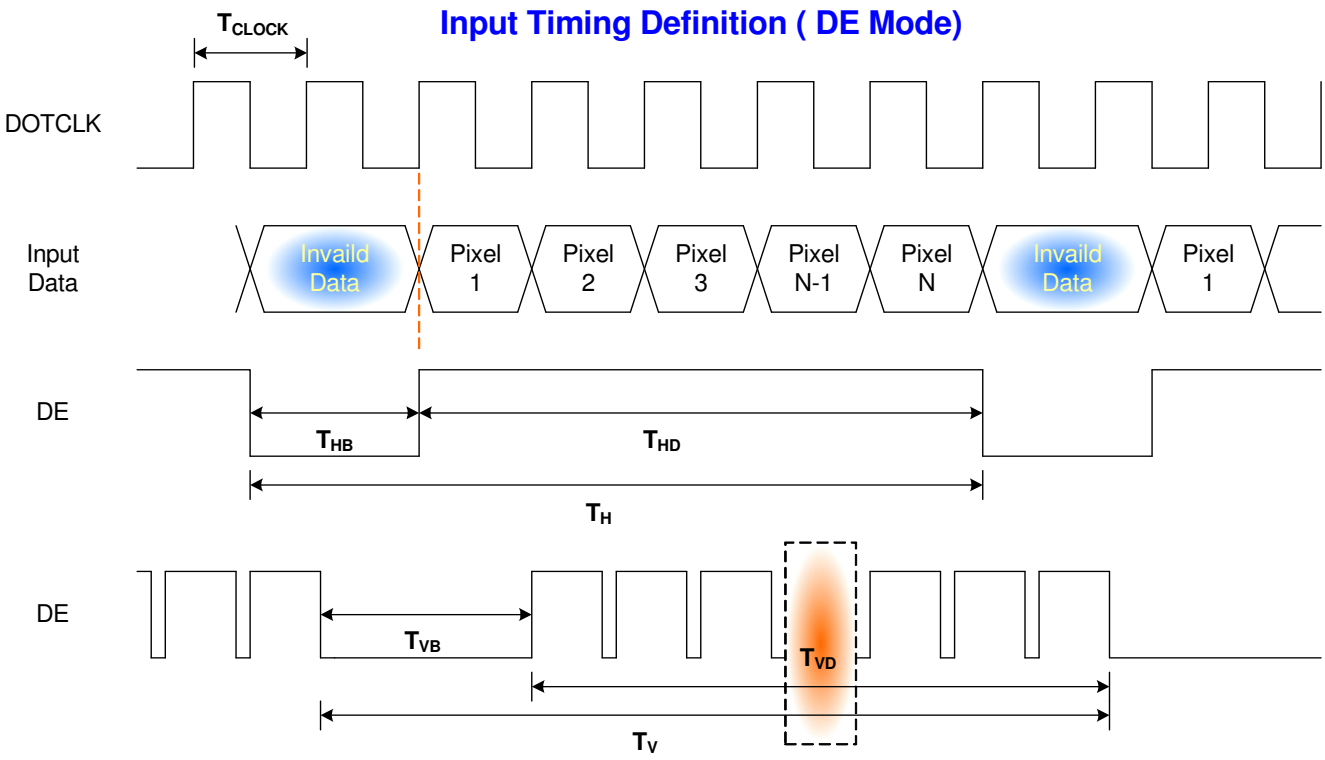
Signal	Parameter	Symbol	Min	Typ	Max	Unit	ote
D_{CLK}	Clock Period	T_C		13.79		ns	1
	Clock Frequency	f_C		72.50		MHz	$1/T_C$
	Duty Ratio (% High)	K_{dr}	40	50	60	%	T_{Ch}/T_C
	Rise Time	$T_{R\ CLK}$	-	4.42	-	ns	
	Fall Time	$T_{F\ CLK}$	-	4.42	-	ns	
DE	DE Setup Time	T_{se}	4	-	-	ns	
(Data Enable	Data Setup Time	T_{sd}	4	-	-	ns	
Only)	Data Hold Time	T_{hd}	2	-	-	ns	
(DTMG)	Horizontal Period	T_H		1440		T_C	2
Data	Horizontal Blank Period	T_{ha}		160		T_C	
	Vertical Period	T_V		823		T_H	f_V=59.94 Hz, 3
	Vertical Blank Period	T_{wvb}		23		T_H	
H_{sync}	H_{sync} Back Porch	H_{bp}		80		T_C	
	H_{sync} Pulse Width	T_{WH}		32		T_C	
	H_{sync} Front Porch	H_{fp}		48		T_C	
	Horizontal Active Period	T_{HD}	1280	1280	1280	T_C	Display Period
V_{sync}	V_{sync} Back Porch	V_{bp}		14		T_H	
	V_{sync} Pulse Width	T_{WV}		6		T_H	
	V_{sync} Front Porch	V_{fp}		3		T_H	
	Vertical Active Period	T_{VD}	800	800	800	T_H	Display Period

Note: (1) When the WXGA+ controller sets DE Mode, and H_{sync} and V_{sync} are required. The duration of DE (DTMG) signal must be longer than 1 clock period (T_C) at every horizontal sync period;

(2) Horizontal Period = One Line Scanning Time;

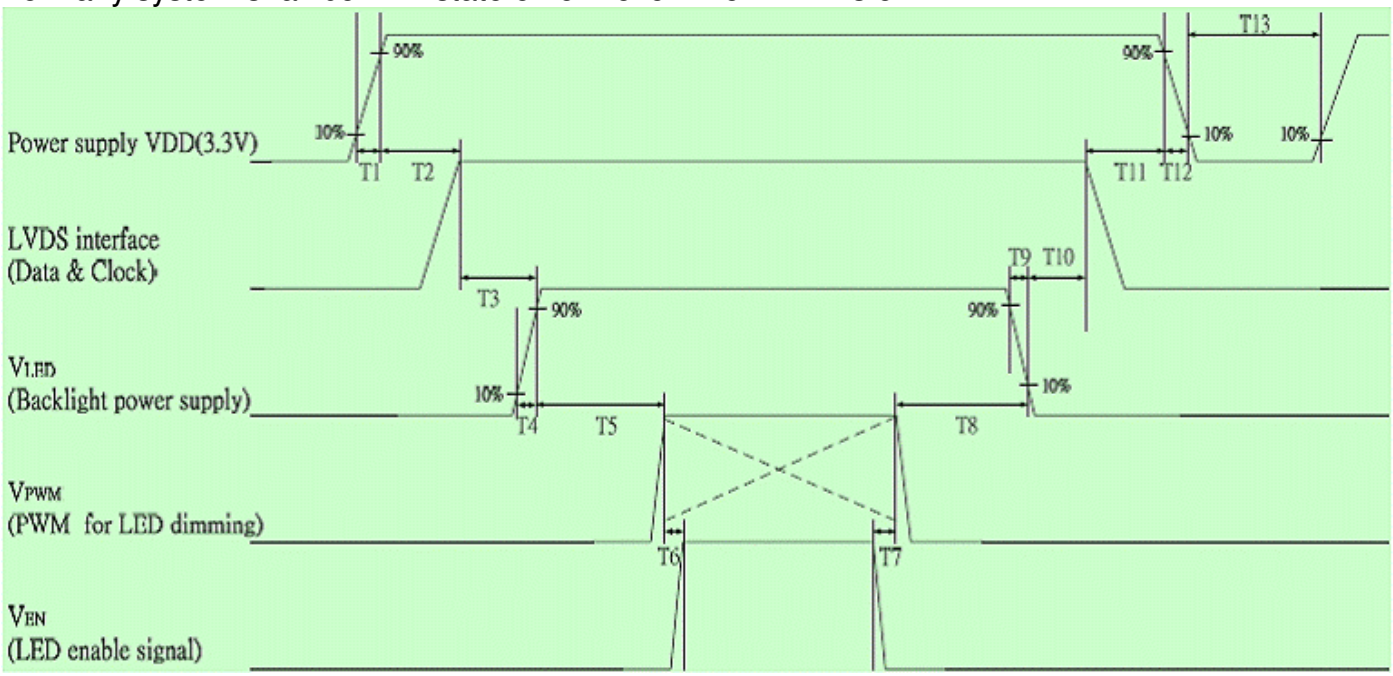
(3) The vertical period T_V is related to the frame frequency f_V, *i.e.*, 60 Hz.

6.4.2 Timing diagram



6.4.3 Power ON/OFF Sequence

VDD power on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off



Power Sequence Timing

Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	ms
T2	0	-	50	
T3	200	-	-	
T4	0.5	-	10	
T5	10	-	-	
T6	10	-	-	
T7	0	-	-	
T8	10	-	-	
T9	0	-	10	
T10	200	-	-	
T11	0.5	-	50	
T12	0	-	10	
T13	400	--	-	

7. Vibration and Shock Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 3 G
- Frequency: 5 - 150Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test Spec:

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

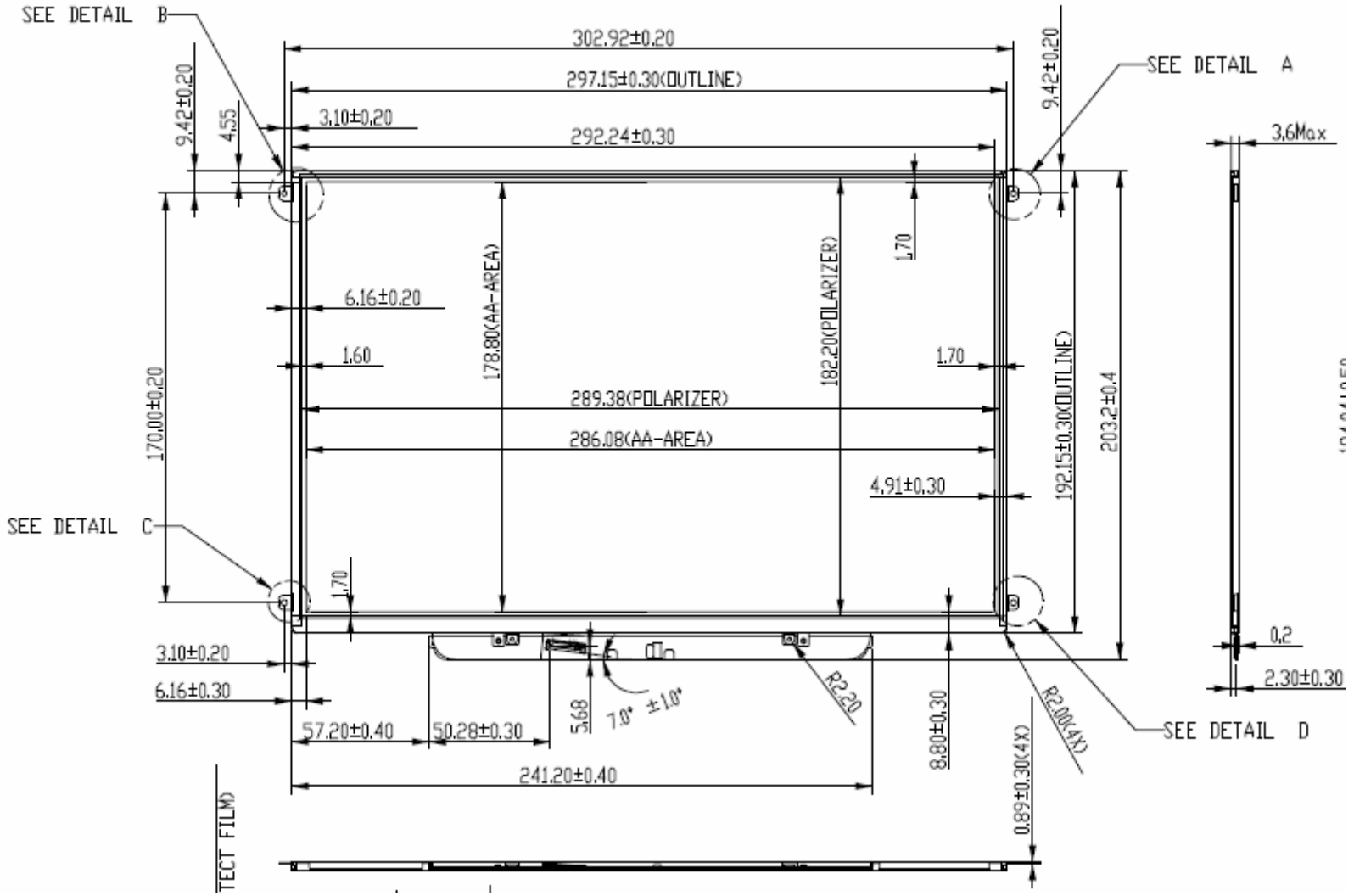
Items	Required Condition	Note
Temperature Humidity Bias	Ta= 50℃, 90%RH, 240h	
High Temperature Operation	Ta= 50℃, 500h	
Low Temperature Operation	Ta= 0℃, 500h	
High Temperature Storage	Ta= 65℃, 500h	
Low Temperature Storage	Ta= -25℃, 500h	
Thermal Shock Test	Ta=-25℃to 65℃, 5min transfer time, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

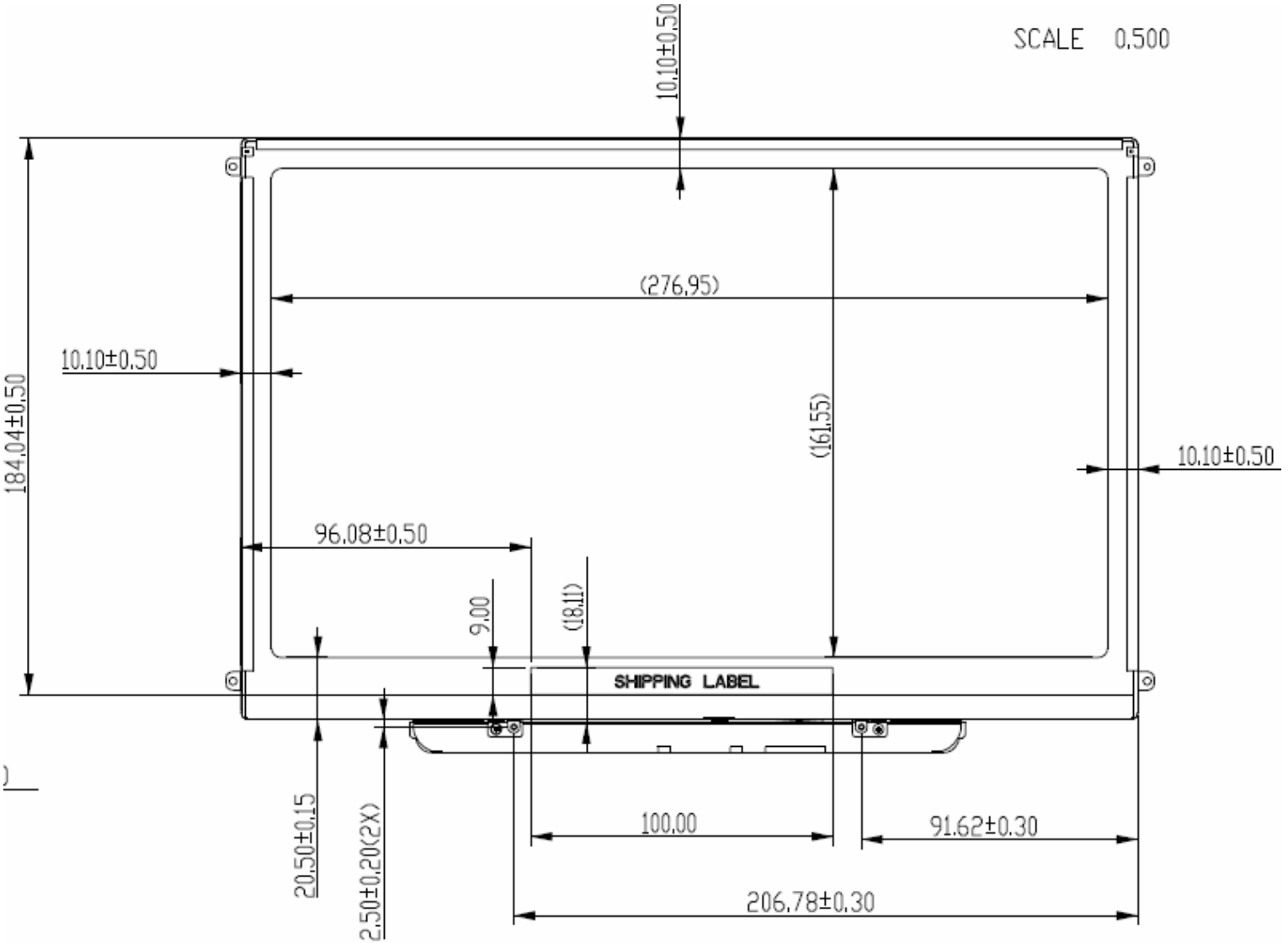
Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost . Self-recoverable. No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

8. Mechanical Characteristics

8.1 LCM Outline Dimension





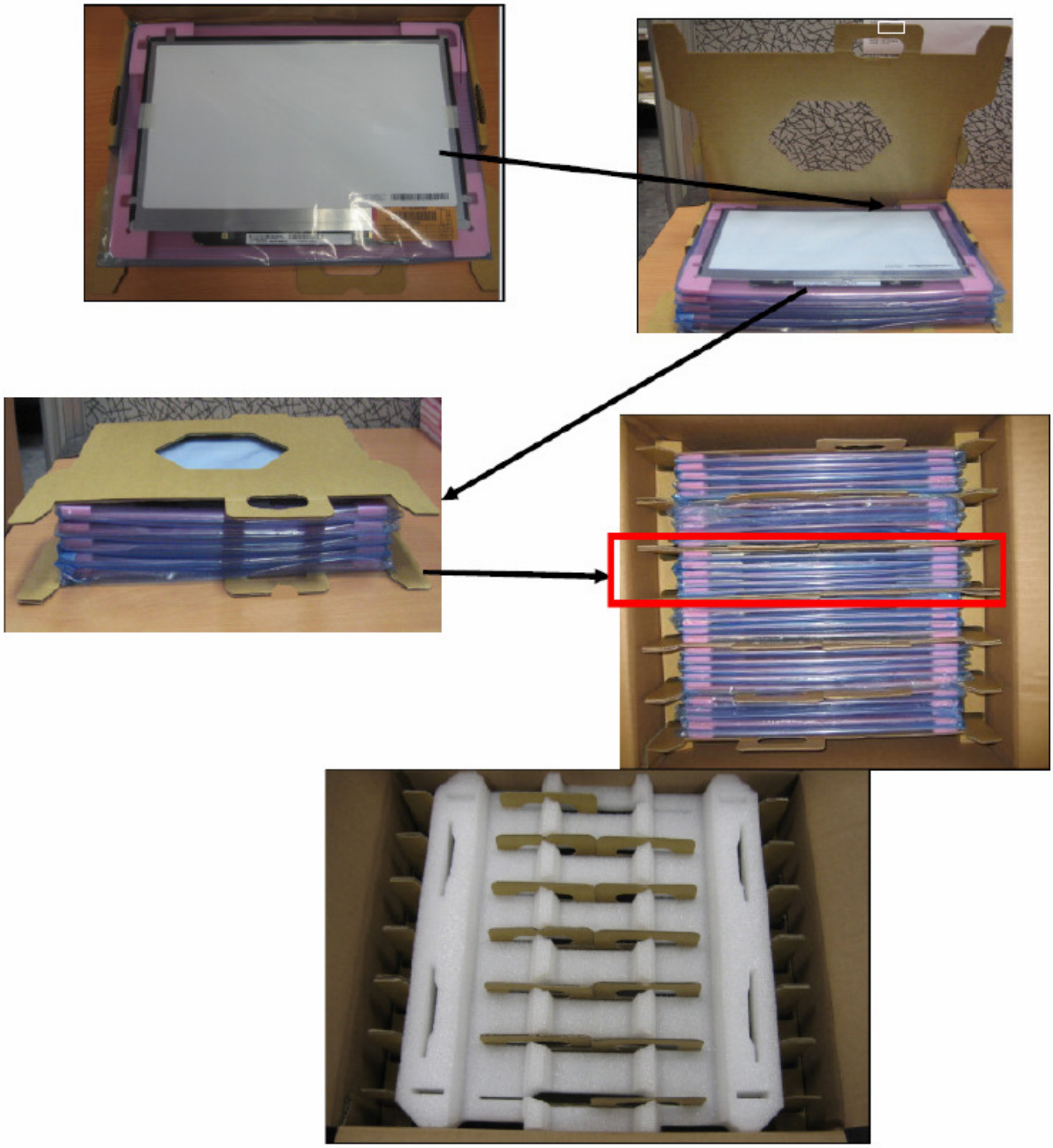
Note: Prevention IC damage, IC positions not allowed any overlap over these areas.

9. Shipping and Package

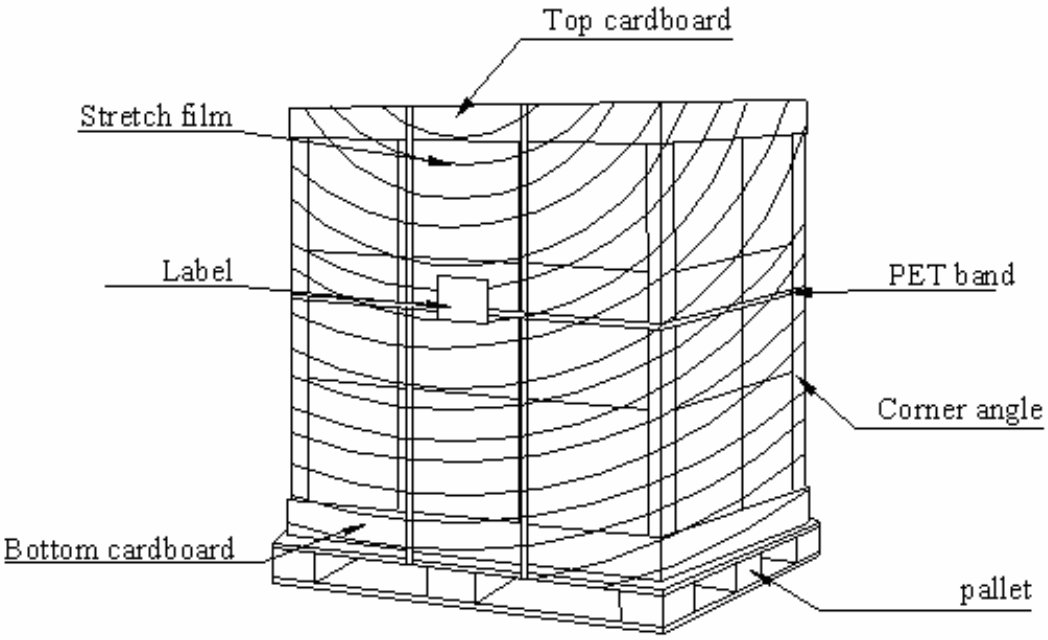
9.1 Shipping Label Format

9.2 Carton package

The outside dimension of carton is 435 (L)mm x 377 (W)mm x 335 (H)mm



9.3 Shipping package of palletizing sequence



10. Appendix: EDID description

2	B133EW07	Value	Value	Note
Header	HEX	BIN	DEC	
	00	00000000	0	
	FF	11111111	255	
	FF	11111111	255	
	FF	11111111	255	
	FF	11111111	255	
	FF	11111111	255	
	FF	11111111	255	
	00	00000000	0	
EISA Manuf. Code LSB	06	00000110	6	APP9CCB
Compressed ASCII	10	00010000	16	0 00001(A) 10000(P) 10000(P)
Product Code	CB	11001011	203	9CCB (apple assigned code)
hex, LSB first	9C	10011100	156	
32-bit ser #	01	00000001	1	unused
	01	00000001	1	
	01	00000001	1	
	01	00000001	1	
Week of manufacture	01	00000001	1	Week 1
Year of manufacture	13	00010011	19	19(2009-1990=19)
EDID Structure Ver.	01	00000001	1	
EDID revision #	03	00000011	3	
Video input definition	80	10000000	128	Digital Input
Max H image size	1D	00011101	29	28.6cm
Max V image size	12	00010010	18	17.9cm
Display Gamma	78	01111000	120	Gamma 2.2
Feature support	0A	00001010	10	no DPMS,Active off,RGB color
Red/green low bits	C5	11000101	197	
Blue/white low bits	95	10010101	149	
Red x/ high bits	A3	10100011	163	Rx=0.640
Red y	57	01010111	87	Ry=0.340
Green x	4F	01001111	79	Gx=0.310
Green y	9C	10011100	156	Gy=0.610
Blue x	26	00100110	38	Bx=0.150
Blue y	0F	00001111	15	By=0.060
White x	50	01010000	80	Wx=0.313
White y	54	01010100	84	Wy=0.329
Established timing 1	00	00000000	0	unused
Established timing 2	00	00000000	0	
Manufacturer's Timing	00	00000000	0	
Standard timing #1	01	00000001	1	unused
	01	00000001	1	

Standard timing #2	01	00000001	1	
	01	00000001	1	
Standard timing #3	01	00000001	1	
	01	00000001	1	
Standard timing #4	01	00000001	1	
	01	00000001	1	
Standard timing #5	01	00000001	1	
	01	00000001	1	
Standard timing #6	01	00000001	1	
	01	00000001	1	
Standard timing #7	01	00000001	1	
	01	00000001	1	
Standard timing #8	01	00000001	1	
	01	00000001	1	
Pixel Clock/10,000 (LSB)	52	01010010	82	**Timing Descriptor #1**
Pixel Clock/10,000 (MSB)	1C	00011100	28	1280x800 @60_mode:pixel clock=72.5MHz
Horiz. Active pixels(Lower 8 bits)	00	00000000	0	Horiz active=1280 pixels
Horiz.Blanking (Lower 8 bits)	8F	10001111	143	Horiz blanking=143pixels
Horiz. Active pixels:Horiz. Blanking (Upper4:4 bits)	50	01010000	80	
	20	00100000	32	Vertcal active=800 lines
	2E	00101110	46	Vertical blanking=46 lines
Vert. Active pixels:Vert. Blanking (Upper4:4 bits)	30	00110000	48	
	30	00110000	48	Horiz sync. Offset=48 pixels
	20	00100000	32	Horiz sync. Pulse Width=32 pixels
Vert. Sync. Offset=xx lines, Sync Width=xx lines	36	00110110	54	Verti sync. Offset=3 lines,Sync Width=6 lines
Horz. Ver. Sync/Width (upper 2 bits)	00	00000000	0	
Hori. Image size (Lower 8 bits)	1E	00011110	30	Hori image size= 286 mm
Vert. Image size (Lower 8 bits)	B3	10110011	179	Verti image size = 179mm
Hori. Image size : Vert. Image size (Upper 4 bits)	10	00010000	16	
	00	00000000	0	Horizontal Border = 0
	00	00000000	0	Vertical Border = 0
	18	00011000	24	
Detailed timing/monitor	00	00000000	0	
descriptor #2	00	00000000	0	
	00	00000000	0	
	01	00000001	1	For apple
Version	00	00000000	0	For apple
Apple edid signature	06	00000110	6	For apple
Apple edid signature	10	00010000	16	For apple
Link Type (LVDS Link,MSB justified)	20	00100000	32	For apple
Pixel and link component format (6-bit panel interface)	00	00000000	0	For apple

Panel features (No inverter)	00	00000000	0	For apple
	00	00000000	0	
	00	00000000	0	
	00	00000000	0	
	00	00000000	0	
	00	00000000	0	
	00	00000000	0	
	0A	00001010	10	
	20	00100000	32	
Detailed timing/monitor	00	00000000	0	ASCII Data String:B133EW07 V2
descriptor #3	00	00000000	0	
	00	00000000	0	
	FE	11111110	254	
	00	00000000	0	
	42	01000010	66	B
	31	00110001	49	1
	33	00110011	51	3
	33	00110011	51	3
	45	01000101	69	E
	57	01010111	87	W
	30	00110000	48	0
	37	00110111	55	7
	20	00100000	32	
	56	01010110	86	V
	32	00110010	50	2
	0A	00001010	10	
	20	00100000	32	
Detailed timing/monitor	00	00000000	0	Monitor Name: Color LCD
descriptor #4	00	00000000	0	
	00	00000000	0	
	FE	11111110	254	
	00	00000000	0	
	43	01000011	67	C
	6F	01101111	111	o
	6C	01101100	108	l
	6F	01101111	111	o
	72	01110010	114	r
	20	00100000	32	
	4C	01001100	76	L
	43	01000011	67	C
	44	01000100	68	D
	0A	00001010	10	
	20	00100000	32	
	20	00100000	32	

	20	00100000	32	
Extension Flag	00	00000000	0	
Checksum	63	01100011	99	
		SUM	6400	